**Laboratory on voltage converters**

**Goals of the experiment:**

* to investigate a switching mode power converter (SMPC) with Buck topology
* to implement a simple control loop based on a PID controller

**Group # \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Date \_\_\_\_\_\_\_\_\_\_\_\_\_\_**

|  |  |
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| **Last Name/First Name** | **Student ID** |
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**Laboratory on voltage converters**

**First experiment**

**Goal of the experiment:** to investigate a switching mode power converter (SMPC) with Buck topology, in open loop

**Circuit schematic:**



**List of components:**

|  |  |
| --- | --- |
| **Tipo componente** | **Codice costruttore/Valore** |
| Switch: MOSFET | IRF630 |
| Gate driver | LTC7001 |
| D: pn diode | 1N4004 |
| RL: Load resistance | 50 Ohm (parallelo di 2 resistenze da 100 W, 1 Watt) |
| L: inductor | To be calculated |
| C: capacitor | To be calculated |

**First experiment: PRELAB**

1. Considering a switching frequency of 50 kHz, and an input voltage =8 V, determine the minimum value of the inductance to guarantee continuous conduction mode for duty cycles higher than 20 % (discuss, with the help of formulas)
2. Choose a proper inductor, from those available in the laboratory

|  |  |
| --- | --- |
| L= |  |

1. Calculate the expected minimum and maximum inductor current and add the results to the report
2. Find a proper value of the capacitance C, to ensure that the output voltage ripple is smaller than 100 mV (discuss, with the help of formulas)

**First experiment: IN THE LAB**

1. Build the circuit, following the schematic below
2. Use the bipolar voltage output on the right of the power supply (channel 2), to generate the 8 V voltage necessary for the circuit



1. Apply a square wave (Vpp= 5V, Voffset=2.5 V, f=50 kHz, duty cycle=50 %) to the INP terminal of the LTC7001
2. Check the voltages on the gate and on the source of the transistor and add the related plots to the report, with a short comment
3. Measure the output voltage across the load resistor R, as a function of time and add the related plot to the report, with a short comment
4. By using the current probe (clamp it on one of the leads of the inductor), measure the current through the inductor during few switching periods. Compare the results to the expected value (point 3, PRELAB)
5. Measure the ripple of the output voltage and add the related plot to the report, with a short comment
6. Measure the dependence of the output voltage on duty cycle, and fill the table below

|  |  |
| --- | --- |
| Duty cycle (%) | Output Voltage (V) |
| 20 |  |
| 30 |  |
| 40 |  |
| 50 |  |
| 60 |  |
| 70 |  |
| 80 |  |

Plot the results in a diagram and add a comment to the report

**First experiment**

**Goal of the experiment:** to investigate a switching mode power converter (SMPC) with Buck topology, in closed loop

**Circuit schematic:**



**Second experiment: PRELAB LAB**

1. Consider now to set C1=20 µF, and use the same values of L1 and R1 used in the first part of the experiment
2. Calculate and plot the Bode diagram of the LRC filter
3. Add a feedback loop, by modifying the circuit as follows (for Vref, use the left CH1 output of the power supply; for powering the op amp use the positive/negative voltage output CH2 and CH3 on the right; set +Vcc=8 V; -Vcc=0 V).

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Description automatically generated

1. Choose proper values for the resistors R6, R7, with the goal of having an output voltage on the load equal Vref); note that the presence of the voltage divider R1, R2 connected to the output will modify the loop gain compared to what seen during the lecture
2. Choose proper values for the capacitors CF and CI (the goal is to have a stable system, as discussed during the lecture; set RF and RI to 10 kW)
3. Connect a 10 µF capacitor in parallel to the supply of the OP amp (between +VCC and ‑VCC)
4. Calculate and plot the Bode diagram of the loop gain, as discussed during the lecture
5. Turn on the circuit and evaluate the behavior, by adding proper plots to the report (for Vref=4 V, plot the output voltage, the signal on the INP input of the LTC7001, the saw-tooth signal, the signal at the output of U1)
6. Measure the dependence of the output voltage on Vref, and fill the table below

|  |  |  |
| --- | --- | --- |
| Vref (V) | Duty cycle (%) | Output Voltage (V) |
| 2.0 |  |  |
| 2.5 |  |  |
| 3.0 |  |  |
| 3.5 |  |  |
| .. |  |  |
| 6.0 |  |  |
|  |  |  |

Plot the results in a diagram and add a comment to the report

1. Future of electronics: why new semiconductors like GaN and SiC are much better than silicon for efficient power conversion in energy efficiency applications (electric cars, photovoltaics, etc.)?